Void Size Process Control During Die Attach of Large Area HIGH POWER Semiconductor Devices

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Abstract: *To realize the full potential of increased power densities from GaAs and GaN devices, a high yielding void free manufacturing process was developed to limit void sizes to less than 0.15mm during eutectic soldering. Voiding between die and thermal spreader can significantly limit thermal heat transfer. GaAs die can handle power densities of 1.0 watt / mm while new GaN devices push this power density to 5.0 watts / mm or greater. Traditional assembly methods for attaching large area GaAs or GaN die to thermal spreaders using Au-20Sn preforms are typically poor yielding due to significant voiding under power FETs and bond pads. Thermal simulations show that voiding greater than 0.15mm under power FET's can seriously reduce performance or in some cases cause catastrophic device failure. Without void size process control, assembly yields are significantly compromised.*

Void control can be significantly improved when using vacuum reflow equipment and a technique to reduce chamber pressure after the solder has transitioned from solid to liquid. Void size expansion is inhibited by a Void Expansion Slip (VES) factor, creating smaller voids and allows large compression ratios at the completion of the solder process. Adding this technique to a vacuum reflow process will produce void free solder yields greater than 98% on very large die.

Keywords: Void free solder process; die attach; eutectic solder process; vacuum reflow; vacuum soldering, void expansion slip (VES).

Introduction

Fluxless eutectic soldering of semiconductor die to thermal dissipating structures is well documented [1][2]. In practice, using these techniques can produce void free results, however overall yields tend to be low. Our focus was centered on 278° C, eutectic Au-20Sn soldering materials. The same principles will apply to all eutectic solder processes.

To achieve a repeatable void free process, all joining materials must be clean, oxidation free with no volatile out gassing components at liquidus solder temperatures; the Au-20Sn preform must be sized to match die and thermal transfer impedance goals; weight selected for desired compressive force; and then apply an optimized vacuum solder process.

Void Free Process Definition

Thermal conduction simulations show that voiding under power FETs must be < 0.15mm in any direction and total voiding < 10%. To improve assembly yields, voids under bond pads must also be limited to <0.15mm in any direction. After the soldering process, real time XRAY was used to identify and measure the size of Au-20Sn solder voids between die and thermal spreader.

Material Prep

Before soldering, the Au-20Sn preform and thermal spreader were cleaned in Isopropyl alcohol, assisted with ultrasonic agitation for 15 minutes and then dried. Thermal spreaders were then vacuum baked at 350° C for 30 minutes to eliminate surface out gassing during the liquidus phase of the assembly process.

Au-20Sn Preform Selection

Die size, external weight and volume of solder will determine overall preform dimensions. Once the die flat dimensions (length, width) have been determined, preform thickness can be adjusted to achieve the desired volume of solder. As long as thermal performance is not compromised, 0.051mm thick preforms are preferred as applications can use smaller external weights and obtain better void control.

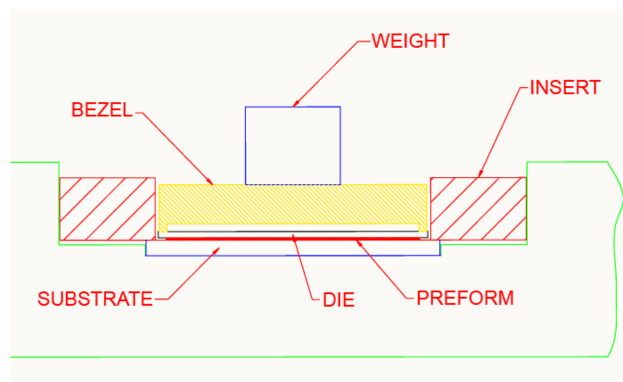

Figure 1. View of Assembly Fixture

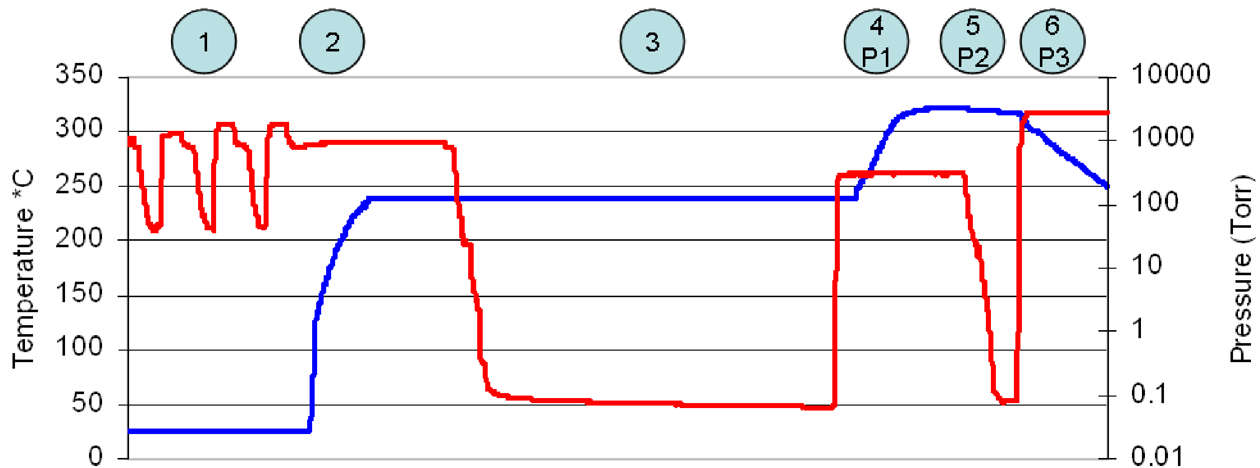

Figure 2. Temperature and Vacuum / Pressure Au-20sn Reflow Profile
Solder Liquid Pressure zones P1, P2 & P3

Die Weight Selection
Applying a compressive force (see Figure 1) to the die during soldering will reduce voiding [1] and improve the solder fillet around the edge of the die. Weight selection is determined by die area, preform thickness, available solder run out perimeter around the die, and voiding criteria. Always select a die weight that will provide a force greater than .05 grams / mm^2. Forces larger than this are preferred if sufficient solder run out perimeter around die is available. Voids created during P1 solder melt will be smaller using larger weights and also improve Void Expansion Slipping (VES).

Vacuum Solder Process
Commercial vacuum solder ovens provide a low oxygen solder environment, high temperature vacuum bake for removal of water vapor and organic residues [2] and help prevent subsequent out gassing from porous materials. These solder ovens are also capable of controlling temperature and pressure independently [2] to significantly reduce voiding. Adding a vacuum Zone #5 (see Figure 2) creates a Void Expansion Slip (VES) factor that scales Boyle's gas law [2][3], the inversely proportional relationship between the absolute pressure and volume of a gas. The VES factor calculated using the solder process shown in Figure 2, reduced void volumes at this step by 535x. This void volume reduction enhances vacuum soldering process and significantly improves overall yields.

Start the solder process by loading the solder assembly fixture into the vacuum reflow chamber (See Figure2).

Step #1: Purge the vacuum chamber several times with high purity nitrogen to displace oxygen.

Step #2: Heat the solder fixture to desired bake out temperature.

Step #3: Pull vacuum for 10 minutes (VAC bake).

Step #4: Increase pressure to 300 torr and then increase temperature rapidly to 320° C. Au-20Sn will transition from solid to liquid (see P1 Zone 4, Figure 2). Assuming no material out gassing, voids are created at this process step and void sizes are determined by the compressive force [1] applied to the die surface. Sufficient chamber pressure must be used to allow adequate thermal transfer from heat source to soldering fixture during fast temperature ramp. Experiments have shown that initial void size formation is not influenced by initial pressure P1 conditions. However in practice, void reduction is enhanced by using the lowest possible P1 pressure that still maintains adequate thermal convection to the solder fixture.

Step #5: Adding this vacuum step (see Figure 2, Zone 5) creates a VES factor that scales Boyle's gas law, the inversely proportional relationship between the absolute pressure and volume of a gas. This VES factor improves overall void volume compression during the vacuum solder process.

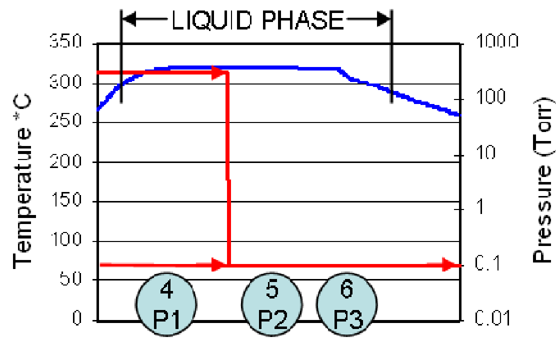

Figure 3. Void Formation Experiment Process Curves

	Pressue (Torr)			Measured Mean Void Volumes		
	P1	P2	P3	Mean (mm^3)	3 sigma (mm^3)	VES Factor
Exp #1	0.1	0.1	0.1	1.66E-03	1.30E-02	1.0
Exp #2	300	0.1	0.1	8.97E-03	6.22E-02	1.80E-03

Figure 4. Void Expansion Slip Table (VES)
4.2 x 4.6mm GaAs Die
0.051mm Solder Preform
10 Devices Processed per Experiment
10 largest voids measured on each die

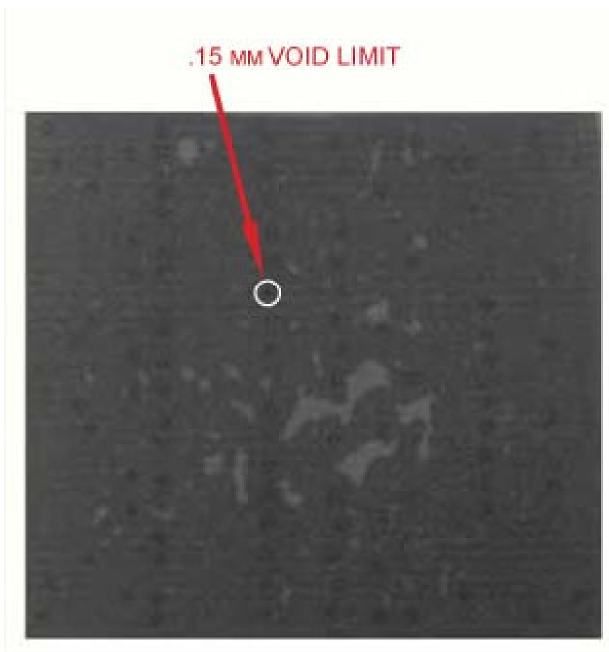

Figure 5. XRAY – Voiding
Constant Pressure Process P1= P2= P3= 0.1 torr, (4.2 x 4.6mm) GaAs Die, process Per Figure 3, super imposed circle illustrates 0.15mm void size limit.

VES can be calculated by first measuring void volumes (see Figure 5) that are created using a soldering process where pressure is held constant P1=P2=P3 in Zones 4, 5 & 6 (see Figures 2 & 3). Then run a second set of devices where P1=300 torr and P2=P3= 0.1 torr in Zones 4, 5 & 6 (see Figure 3) and measure void volumes (see Figure 6 and also experimental data provided in Figure 4). Void reduction improvement of the system is inversely proportional to VES.

$$VES = \frac{Vm2}{Vm1} \times \frac{P2}{P1}$$

Vm1 = Mean void volumes from Exp #1
Vm2 = Mean void volumes from Exp #2
P1 = Pressure Zone 4
P2 = Pressure Zone 5

Using data from Figure 4,

$$VES = \frac{.00897\ mm^3}{.0016\ mm^3} \times \frac{(\ 0.1\ torr)}{(\ 300\ torr)} = .00187$$

$$\text{Void Improvement of Solder System} = \frac{1}{VES} = 535 \text{ times}$$

Combine Boyle's law P1V1=P2V2 [2, 3] and Void Expansion Slip (VES) factor to create this relationship

[VES x P1 x V1] / P2 = V2

Figure 6. XRAY – Voiding
P1= 300 torr, P2=P3= 0.1 torr
(4.2 x 4.6mm) GaAs Die
Process Per Figure 3

P1 = Initial chamber pressure
P2 = Chamber Zone 5 (see Figures 2 & 3)
V1 = Initial void volumes
V2 = Void volumes created at Step # 5 (Zones 5, see Figures 2 & 3)
VES = Void Expansion Slip

Void Expansion Slip (VES) factor is influenced by compressive die force, die size, preform thickness and ratio of pressure decrease P2 / P1. If device or process parameters change, new process experiments need to be run followed by calculation a new system VES factor.

Ten die were processed according to the process diagram in Figure 3, P1=P2=P3 at 0.1 torr and die with largest voids presented in Figure 5. Voids created using this constant pressure process are similar to traditional belt furnace processing. Using only compressive force on the die surface is not very effective at eliminating voids.

Step #6: While solder is still liquid, pressurize chamber to 2,824 torr (Pressure Zone 6). Low to high pressure change P2 to P3 (refer to Figure 2, zone 5 & 6) will cause voids to decrease in size expressed by: P2V2=P3V3

P3 = Chamber pressure Zone 6
V3 = Final void volume

Overall void size reduction:

$$V3 = \frac{VES \times P1 \times V1}{P3} = 533\text{x Improvement}$$

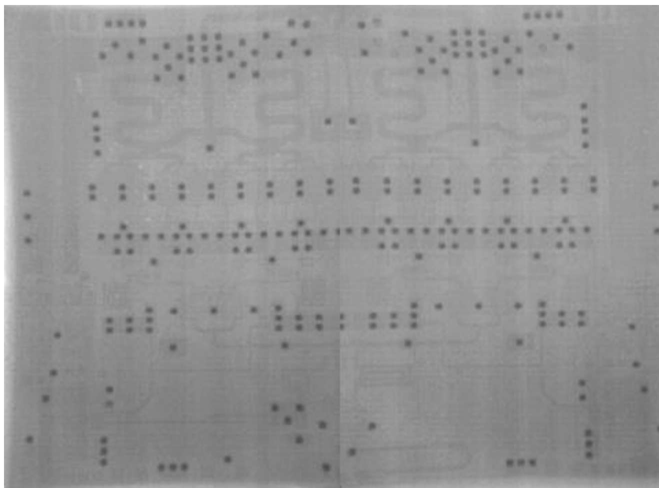

Figure 7. 100% Void Free Die Attach (8 x 6.5mm) GaAs Die, preform outline same as die with thickness 0.051mm, die weight 4 grams. Two XRAY images stitched together to form complete image

Results
XRAY shown in Figure 7 illustrates an example of a Void Free process for a large 8x6.5mm GaAs die.

Three lots of material were processed using vacuum solder process presented in this paper. Void defects are controlled and most importantly process yields are very high.

Run #	Devices Processed	Yield	% Yield	Dice Size
1	61	61	100.0%	4.2 x 4.65mm
2	232	228	98.3%	4.2 x 4.65mm
3	7	7	100.0%	6.5 x 8mm

Figure 8. Process yields for devices within void criteria. Preform outline same as die, preform thickness 0.051mm. Runs #1 & 2 die weight 1 gram, run 3 die weight 4 grams

Units that failed the stated void free process definition were caused by:
1) Incomplete void collapse during P2 to P3 transition by higher temperature AuSn4 precipitates that restricted solder flow
2) Voids caused by out gassing of foreign material in GaAs VIA's during pressurization Step #6 (Figure 2).

Summary:
1) Material must be clean; no oils or foreign material.
2) 0.051mm thickness preforms are preferred as long as thermal performance is not compromised.
3) Use die weights to provide compressive force.
4) Use vacuum solder process.
5) Add VES vacuum process step to further reduce voids using standard vacuum reflow equipment.
6) Total voiding should be < 0.5%
7) Overall yield due to voiding > 98%

Acknowledgements
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