Engineering:  
Criteria Labs has assembled world-class design and engineering teams to solve your complex problems.

TURNKEY
- Product engineering
- Program management
- Advanced interconnect development
- Packaging and development of interconnecting technologies
- Process development for advanced technology
- Qualification plan development
- Construction analysis
- Semiconductor failure analysis

SOFTWARE
- Characterization and validation of new silicon (digital, mixed signal, discrete components, i.e. transistors, diodes and RF)
- Test plan and design for testability, probe and final test (digital, mixed signal, discrete components, i.e. transistors, diodes and RF)

HARDWARE
- Test analysis for yield improvement
- Test analysis for test time reduction
- Conversion between different ATE platforms (digital and mixed signal)

PROCESS ENGINEERING FOR MICROELECTRONIC PACKAGING
- Probes
- Load board design (low frequency to high frequency)
- Burn-in/HAST board design
- DUT/probe interface boards
- Tape pocket design (for tape & reel services)
- Handler kit/interface

Fabless Semiconductor Companies or JEDEC Plastic Services and Commercial

Criteria Labs provides all back-end semiconductor services required by our fabless semiconductor customers. We provide full test engineering development service, device qualifications, reliability analysis, tape & reel and technology transfer. Whether you need just one of our world-class services or full turnkey capability, Criteria Labs wants to be a partner in your success.
Services:
Criteria Labs provides a broad array of in-house services to reduce your time to market, verify quality and make sure what you’re shipping meets your exact specifications.

WAFFER TEST, FINAL TEST and TEST ENGINEERING SERVICES
- Wafer probe from -55º C to +175º C
- Off line inking
- Final semiconductor package electric test -55º C to +175º C
- Wafer mapping
- Data logging and yield monitoring with feedback to customer
- Laser marking
- Package inspection

DIE PROCESSING
- Wafer saw (2” to 8”)
- Wafer sort
- Visual inspection (MIL-STD 883 Method 2010 A or B)
- Die mapping
- Wafer wash/ink removal
- Die sort duals, trios and quads
- Die to waﬄe pack/GEL pack
- Die to tape
- Bar code labels
- Special packing

PACKAGING
COMMERCIAL, MEDICAL CUSTOM, CERAMIC AND PROTOTYPE
- Ceramic dips, ﬂat packs, LCC, CERQUAD, CERPAC, ceramic SOIC
- BGA, CQFP, CPGA, TO-CAN, METAL CAN
- Sidebraze, JLCC
- Multi-chip module (MCM), hybrids, chip on board (COB)
- Flex assembly, smart cards, FR4 chip bonding
- MIMS assembly
- Opto assembly
- Die attach material
  - Silver glass: QMI 2569 conductive
  - Silver-ﬁlled cyanate ester: JM-7000 and QMI-84-1 or 3 (conductive or nonconductive)
  - Silver-ﬁlled epoxy
  - Electrically insulating epoxy
  - Low-temp cure epoxies
  - Eutectic:
    - 2% silicon 98% gold preform
    - 80% gold 20% tin preform
- Sealing and encapsulation
  - Solder sealing (gold-tin eutectic) and glass sealing
  - Resistance welding for metal cans
  - Glob topping with hysol material on custom packages
  - Seam seal
  - Taped lids
  - B-stage epoxy attachment
- Assembly testing (quality conforms or exceeds JEDEC/military requirements)
  - Die shear strength
  - Bond pull
  - Non-destructive bond pull (Class S)
  - Fine and gross leak testing
  - Constant acceleration (centrifuge)
  - Solderability
  - Temperature cycle
  - Resistance to solvents
  - External visual
- Lab suitability qualification services
  - Solder dip
  - Lead trim and form/manual
  - Lead inspection and repair
  - Temperature cycle
  - Constant acceleration (centrifuge)
  - Fine and gross leak
  - Resistance to solvents testing
  - Marking
**PRODUCT ASSEMBLY STRESS SCREENING FOR PLASTIC DEVICES**

> Environmental Tests
- Steady state life test
- Temp cycling
- Burn-in

> Mechanical Tests
- Physical dimensioning
- Marking: stamp or laser
- Adhesion of lead finish
- Lead integrity
- Lead torque
- Lid torque for glass fit sealed packages
- Visual

> Process Testing
- Latch up/electrical overload stress (EOS)
- Electro static discharge (ESD) HMB, MMB and CDM

**PRODUCT QUALIFICATION TESTING FOR PLASTIC ENCAPSULATED DEVICES**

(JEDEC AND AEC STANDARD USED IN AUTOMOTIVE APPLICATIONS)

> Environmental Tests
- Pre-conditioning of plastic surface mount devices prior to reliability testing (Method A113)
- Moisture sensitivity test for plastic surface mount devices (Method A112)
- Lead-free re-flow charting and validation to JEDEC-22 or Japanese automotive requirements (green mold compound)
- Temperature cycling (Method A104)
- Steady state life test/1000 hour burn-in (Method 108A)
- Temperature humidity bias testing (Method A101)
- Autoclave – accelerated moisture resistance – unbiased (Method A102)
- Moisture resistance
- Thermal shock (Method A106)
- Highly accelerated temperature and humidity stress test (HAST) (Method A110)
- High-temp storage (HTS)
- Salt atmosphere (Method A1107)
- High-temp operating life (HTOL) (biased/unbiased)
- THB 85° C/85% RH

> Mechanical Tests
- Physical dimensions (Method B100)
- Vibration, variable frequency (Method B103)
- Mechanical shock (Method B104)
- Lead integrity (Method B105)
- Solderability (Method B102)
- Resistance to soldering heat (Method B106)
- Resistance to solvents (Method B107)

> Process Testing
- Latch up/electrical overload stress (EOS)
- Electro static discharge (ESD) HMB, MMB and CDM

**RELIABILITY ANALYSIS OR FAILURE ANALYSIS**

> Acoustic microscopy (CSAM)
> Focus ion beam (FIB)
> Scanning electron microscope (SEM)
> X-ray
> Real-time X-ray
> Cross sectioning
> Micro-probe
> Light emission microscopy
> De-cap (wet) manual/acid jet etcher
> Construction analysis
> Parallel polishing
> Back lapping
> Latch up/electrical overload stress (EOS)
> Electro static discharge (ESD)
> Level 1, 2 and 3 failure analysis
> EDX
> Digital image capture
> Solderability testing
ELECTRONIC DEVICE PHYSICAL EVALUATION AND ANALYSIS
> BGA and uBGA automatic ball inspection
> Bond pull
> Die shear
> Solder dip
> Lead trim
> Lead inspection and repair
> Solderability restoration
> Bake and dry pack

TAPE & REEL SERVICES
> Tray to tape, QFP, TSOP, BGA, uBGA, FBGA, QFN
> Tube to tape, SOIC, PLCC, SQJ, SOMC, SSOP, TSSOP, MSOP, VSOP, QSOP, QVSOP, DDPAK, DPAK, TO263, PLCC SOCKETS, MLF, MLP
> Bulk to tape SOT, CHIP RESISTORS/CAPACITORS
> Tray to tray
> Tube to tube
> Lead scan trays
> Lead scan tubes
> 3-D laser scanning: QFP, TSOP, BGA and uBGA
> 3-D vision system : SOIC, TSSOP, SSOP, MSOP, VSOP, QSOP, QVSOP, SOMC
> 2-D: QFP, TSOP, PLCC, BGA and uBGA
> Lead conditioning
> In-line mark inspection
> Parts marking
> Tape custom packages (Criteria Labs will custom design tape pocket)
> Bar coding and custom bar coding
> Labeling and custom packaging
> Laser mark capability
> Detape
> Bake and dry pack

QUALITY SYSTEMS
> Total Quality Management Program
> Incoming inspection of consigned and turnkey products
> 100% ESD controlled environment
> Packaging process to customer specifications
> QA sample inspection or 100% based on customer requirements
> SPC controlled in critical processes
> 8D corrective action
> Employee training and certification
> Equipment calibration schedule
> Document control
> Final gate inspection (AQL or LTPD)
> CFC and summary data reports

CERTIFICATIONS and COMPLIANCE PROCESSES
| ISO-9001/2000 |
| QML-PRF-38535 Certified |
| MIL-STD-883 Certified |
| IPC 610 Class I, II, III Certified |
| MIL-PRF-19500 Compliant |
| MIL-STD-750 Compliant |
| Classified Facility Controls |
| EIA 485 Compliant |
| EIA 481 Compliant |

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